ers **92–94**, and making some additional adjustment, if necessary. Here, it is supposed that Vr=Vdd/2=Vb (Vdd signifies the supply voltage) so that the dynamic range can be enlarged. Therefore, when Vr is output from the H-output or the L-output of **73-1** to **73-6**, the input voltage V(i) in formula (2) is 0.

The outputs from MUX1 (H-output) in **73-1** to **73-3** are input to adder **76**. In **76**, as the size of input capacitances C**2**, C**3** and C**4** which correspond to the output voltage from **73-1** to **73-3** are ⅓ that of Cf, the voltage is output with ⅓ the value of the sum of output voltage from **73-1** to **73-3** from formula (2). The polarity of the output voltage is the same as that of input voltage Ri (Rq) of the matched filter.

To adder **78**, H-outputs of **73-4** to **73-6** are input. As with adder **76**, the voltage with the same value as the sum of theirs is output from **78**. The polarity of this voltage is the same as that of Ri (Rq).

The outputs of **76** and **78** are input to adder **80**. The values of input capacitances C**5** and C**6** in **80** are ½ that of Cf. Adder **80** outputs the voltage with the value of the sum of ½ of the outputs from **76** and from **78**. This voltage has reversed polarity from that of Ri (Rq).

On the other hand, the outputs from MUX2 (L-output) in **73-1** to **73-3** are input to adder **77**, from which the voltage with the same value as the sum of theirs is output, as with adder **78**. The L-outputs from **73-4** to **73-6** are input to **79**, from which the voltage is output with the same value as the sum of theirs and with the same polarity as that of Ri (Rq).

The outputs of **80**, **77** and **79** are input to **81**. In **81**, the size of input capacitance C**7** corresponding to the input from **80** is the same as that of Cf, and the sizes of input capacitances C**8** and C**9** corresponding to the input from **77** and **79**, respectively, are Cf/2. Therefore, **81** outputs the voltage with the value of the difference between **80** and the sum of the halves of output voltages **77** and **79**. That is, from **81**, the difference between the sum of the outputs from **71-1** to **71-6** to which spread code sequence 1 is supplied by **75** and the sum of the outputs to which 0 is supplied is output. This means that the correlation value between spread code sequences is output from **81**.

The reason why ½ of the input voltage sum is output from **80** and ½ of the output voltages from **77** and **79** are added is that the maximum voltage does not exceed the supply voltage.

In this matched filter, after the correlation value is output from **81**, the spread code sequence output from **75** is shifted by one chip, and the next correlation value is obtained by performing computation similar to that above. Since it is thus unnecessary to shift the signal performed sampling and holding, no errors caused by shifting occur. Acquisition is completed by sequentially shifting spread code sequences.

This matched filter largely reduces the circuit size compared to digital processing because the computation by the neural operational amplifier is analogously executed using capacitive coupling; also, parallelly processing enhances processing speed. Further, very low electric power consumption is realized since all the inputs and outputs are voltage signals.

Although signals through QPSK processing are exemplified in the above embodiment, another modulation system such as BPSK can also accomplish the processing.

The initial acquisition scheme of the present invention completes a rapid initial cell search because it detects long-code timing using a matched filter, and parallel correlators identify the long code with the detected long code timing.

Also, handover can be realized because the long code timing through handover is detected and the long code through it is identified by a matched filter while the peripheral cell search is carried out, the signal from the base station under communication is received by a correlator, and the signal from the base station through handover can be received at the same time.

RAKE receiving performed by parallelly setting a plurality of correlators allows good signal quality even when multipath fading exists.

Moreover, during the initial cell search, handover and communication (multipath receiving), the matched filter and a plurality of correlators can be commonly used, thus realizing higher efficiency and smaller sizes.

Finally, the receiver affords low electric power consumption by using a matched filter in which a neural operational amplifier is set to work.

What is claimed is:

1. An acquisition scheme for an asynchronous DS-CDMA cellular communication system, using spread code sequences having a long code peculiar to each cell and a short code corresponding to each communication channel, and a control channel among said communication channels employing a specified short code common to each cell, with

(a) two steps for accomplishing the initial cell search:

(1) detecting a correlation between said specified short code and a received signal, and detecting a long code timing of a relevant base station according to the maximal value of correlated outputs, and

(2) identifying a long code of said base station through parallel detection of said long code used in the relevant system, by using a plurality of parallel correlators, or using both said plurality of correlators and a matched filter according to said detected long code timing; and

(b) two steps for accomplishing a peripheral cell search:

(1) detecting a correlation between said specified short code and received signal, and detecting a long code timing of a relevant base station according to correlated outputs, and

(2) identifying said long code of said base station through handover by sequentially detecting a correlation with a long code corresponding to a peripheral cell using said matched filter while communication is continued with the present cell by employing said plurality of parallel correlators according to said detected long code timing, or by sequentially detecting a correlation with a long code corresponding to a peripheral cell using said plurality of correlators while communication is continued with the present cell by employing said matched filter.

2. A receiver for an asynchronous DS-CDMA cellular communication system using spread code sequences having a long code peculiar to each cell and a short code corresponding to each communication channel, and employing a specified short code common to each cell in the receiver's control channel, comprising:

i) a matched filter for detecting a correlation between a received signal and a spread code sequence;

ii) a plurality of correlators parallelly set for detecting a correlation between said received signal and spread code sequence;

iii) a long code timing detector for detecting the maximal correlated output of said matched filter;

iv) a long code synchronization judging means for receiving said correlated output from said matched filter;

v) a long code synchronization judging means for receiving said correlated output from said plurality of correlators;